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Claims

1. A system for integrated circuit design comprising:

a high level design comprising a chip architecture, a floor plan, and one or more critical interconnect wire topologies;

a schematic design comprising one or more circuit components and one or more critical interconnect wire models;

a physical layout comprising said one or more circuit components and said one or more critical interconnect wire topologies;

extracted parameters of said one or more circuit components and calculated parameters of said critical interconnect wire models; and

results of a simulation of a schematic design comprising said extracted parameters and said calculated parameters.

- An integrated circuit design kit comprising:
 one or more circuit components topologies; and
 one or more critical interconnect lines topologies.
- 3. The kit of claim 2 wherein said interconnect line topologies are predefined.
- 4. The kit of claim 2 and further comprising one or more circuit components models.

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- The kit of claim 2 and further comprising one or more critical interconnect lines models.
- 6. A topology of critical interconnect lines.
 - 7. The topology of claim 6 wherein said topology is predefined.
 - 8. The topology of claim 6 comprising a definite current return path.
 - 9. The topology of claim 6 wherein said topology is supplemented by a model comprising one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters.
 - 10. The topology of claim 6 wherein said sum of said currents of a cross section of said topology is zero.
 - 11. The topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires.
 - 12. The topology of claim 11 wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires.



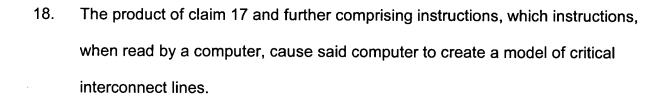
- 13. The topology of claim 11 and wherein said one or more shielding wires is a bottom shielding wire.
- The topology of claim 11 and wherein said one or more shielding wires is one or more shielding layers.
 - A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a topology of critical interconnect lines.
 - 16. The product of claim 15 and further comprising instructions, which instructions, when read by a computer, cause said computer to create a model of critical interconnect lines.
 - A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a design kit comprising a topology of critical interconnect lines.

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- 5 19. A method for designing integrated dircuits (IC), said method comprising the steps of:
 - (a) defining a chip architecture and a floor plan;
 - (b) identifying one or more critical interconnect lines, and defining transmission line topologies for design of said critical interconnect lines;
 - (c) determining a schematic design of said IC;
 - (d) defining a physical layout of said IC;
 - (e) extracting electrical parameters of said layout;
 - (f) simulating said schematic design; and
 - (g) receiving results of said simulation
 - 20. The method of claim 19 and further comprising:
 - (h) comparing said simulation results to a set of initial design requirements.
 - 21. The method of claim 20 and further comprising: according to results of said step (h), repeating steps (d) to (g)
 - 22. The method of claim 19, wherein said integrated circuits are analog and mixed signal (AMS) circuits or application specific integrated circuits (ASIC).

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- 23. The method of claim 19, wherein in (b), the step of defining comprises choosing from a set of predefined parameterized topologies.
- The method of claim 19, wherein in (b), the step of defining comprises defining a set of topologies.
 - 25. The method according to claim 19, wherein said schematic design comprises models of said one or more transmission line topologies.
 - 26. The method according to claim 25, and further comprising the step of calculating one or more electrical parameters of said models.
 - 27. The method according to claim 26, wherein said one or more electrical parameters includes one or more of the following: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters.
- 28. The method according to claim 19, wherein step (b) comprises:
 using one or more of said following to identify said critical interconnect lines:
 estimated length, metal level assignment and manual user selection.

- The method according to claim 19, and further comprising creating parameterized cells from said models.
- A method for designing integrated circuits wherein defining said chip 30. architecture and a floor plan comprises defining critical interconnect wires. 5

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